UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,197	01/28/2004	Douglas L. Youngblood	INSL.0083	3357

26122   7590   08/08/2007
LAW OFFICES OF GARY R. STANFORD
330 W OVERLOOK MOUNTAIN RD
BUDA, TX 78610

EXAMINER
LAO, LUN YI

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
08/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/766,197	YOUNGBLOOD ET AL.
	Examiner	**Art Unit**	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>11 July 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-22</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-5 and 8-22</u> is/are rejected.

7)☒ Claim(s) <u>4-8</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>28 January 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1, 9-15 and 18-22 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Kudo et al(7,023,458) in view of Kato(US 20020126112).

As to claims 1, 9-14 and 18-22, Kudo et al each a gamma correction circuit

comprising: a resistor ladder(307 or 1202)(see figures 3, 12, 13; column 7, lines 44-59;

column 17, lines 18-59 and column 18, lines 5-52) coupled to a reference voltage(316);

a plurality of adjustable resistors distributed along the resistor ladder and providing a

plurality of selectable tap voltages(see figures 3, 12, 13 and column 7, lines 44-59));

a programmable non-volatile memory that stores at least one digital gamma value(see

figures 3, 9, 12-16; column 7, lines 30-43; column 15, lines 7-68 and column 16, lines

1-12); select logic(304-306, 308-313 or 1204, 1205 or 1301-1306) for selecting

resistance value of the variable resistor based on the digital information stored in the

memory, coupled to the memory and to the plurality of adjustable resistors, that selects

each of the selectable tap voltages according to the at least one digital gamma

value(see figures 3, 12-13; column 7, lines 44-68; column 8; column 17, lines 4-68 and

column 18, lines 1-59); and a plurality of buffers(314) having inputs receiving selected

tap voltages and outputs that provide a plurality of gamma correction voltages(see

figures 3, 12-13 and column 7, lines 44-59).

Kudo et al fail to disclose a tap resistor and an integrated circuit.

Kato teach a multiple channel programmable gamma correction voltage

generator comprising a tap resistor(20 or 40)(see figures 3, 5 and paragraphs 31-32

and 71) an integrated gamma correction circuit(see figure 2 and paragraph 28). It

would have been obvious to have modified Kudo et al with the teaching of Kat, so as to

reduce the number of connecting wires, ensure more stable correction and reduce the

dimensions and weight of the LCD device(see paragraph 28).

As to claims 9 and 18, it would have been obvious to have a set of latches with

an external load coupled to the memory device and providing the select values to the

select logic since Kudo et al has disclosed an interface(907) with external load

coupled to a memory device(301) and providing the select values to the select

logic(306, 308-313 or 1204 or 1205)(see figures 3, 9, 12-13; column 7, lines 33-43 and

column 15, lines 2-25).

As to claim 10, Kudo et al teach memory device(301) stores a plurality of sets of

select values, each corresponding to a different gamma correction value, and wherein

the memory device(301) includes an address control input for selecting from among

the plurality of sets of select values and loading the set of latches(figures 3, 9, 12-16;

column 7, lines 44-68; column 8; column 17, lines 4-68 and column 18, lines 1-59);

As to claim 13, Kudo et al teach each of said M buffers(314)comprises an operational amplifier configured as a voltage follower(see figure 3 and column 7, lines 44-59).

As to claim 15, Kudo et al as modified teach a plurality of adjustable tap resistors comprising a plurality of resistors(1R) coupled in series and forming a plurality of junctions and switch logic(704-706) selects one of plurality of junctions(see figures 3, 7A, 7B; column 13, lines 25-68 and column 14, lines 1-22).

As to claim 21, Kudo et al teach the imaging device comprises an LCD panel(see figures 3, 9 and column 14, lines 59-67).

As to claim 22, Kudo et al teaches control logic(906) coupled the memory(301) via address control, wherein the control logic(906) enables selection of a plurality of digital gamma values stored in the memory(301)(see figures 3, 9; column 7, lines 31-43 and column 15, lines 2-59).

3.   Claims 2-5 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable Kudo et al(7,023,458) in view of Kato(2002-0126112) and Suzuki et al(6,157,335).

As to claims 2-5 and 16-17, Kudo et al as modified fail to disclose each of P-1 switch having a first terminal coupled to one of P-1 intermediate junctions.

Suzuki et al teach a circuit having an adjustable tap resistors(R3a-R3h) and (P-1) switches(Sw1-SW8)(see figures 4, 8). Each of the (P-1) switch having a first terminal coupled to one of P-1 intermediate junctions(e.g. N1) (see figures 4, 8 and column 6, lines 20-58). It would have been obvious to have modified Kudo et al as

modified with the teaching of Suzuki et al, so as to easy and accurate to select different

resistance values and output voltages values(see column 2, lines 26-41).

As to claims 2 and 16, Kudo et al as modified by Suzuki et al teach a plurality of

first resistors distributed along the resistor ladder, each coupled to a corresponding one

of the plurality of adjustable tap resistors, each first resistor comprising: a plurality of

second resistors(R3a-R3h), coupled in series forming a plurality of first junctions; and

first switch logic(SW1-SW8) that inserts the corresponding one of the plurality of

adjustable tap resistors at one of the plurality of first junctions(see Kudo's figures 3, 7

and Suzuki's figures 4, 8 and column 6, lines 20-58).

As to claim 3, Suzuki et al teach select logic includes decoder logic(23) which

closes one of the P-1(P is greater than 2) switches of each of the M(M is greater than

1) adjustable tap resistors to select each of the M tap voltages based on a

corresponding one of M select values from the memory device(see figures 4 and

column 6, lines 26-53).

As to claim 4, Kudo as modified by Suzuki teaches a decoder

logic(23)comprises M decoders, each receiving a corresponding one of said M select

values and selecting a corresponding one of the P-1(P is greater than 2) switches of a

corresponding one of the M adjustable tap resistors(see figures 4 and column 6, lines

26-58).

As to claim 5, Kudo et al as modified teaches a resistor ladder(e.g. 307) includes

M+I first resistors(e.g. 322) evenly distributed along the resistor ladder forming M

intermediate locations; wherein at least M of the first resistors each comprise Q

second resistors(1R)coupled in series forming Q-1 intermediate locations and an end

location; wherein the select logic comprises Q switch sets(704), each coupled between

a respective pair of the second resistors(1R) at a corresponding one of the Q

intermediate locations and the end location; and wherein each of the switch(704)sets

is operative, when selected, to decouple the Q second resistors(1R) at a

corresponding one of the Q-1 intermediate locations and said end location and

to insert a corresponding one of the M adjustable tap resistors(see Kudo et al's figures

3, 7, 12-13).

As to claim 17, Kudo et al as modified by Suzuki et al teach each of the plurality

of adjustable tap resistors comprises: a plurality of third resistors coupled in series and

forming a plurality of second junctions; and second switch logic that selects

one of said plurality of second junctions; and the select logic providing a gross

adjustment to each said first switch logic and a fine adjustment to each the second

switch logic(see Kudo's figures 3, 7 and Suzuki's figures 4, 8 and column 6, lines 20-

58).

Allowable Subject Matter

4.   Claims 6-8 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

Response to Arguments

5.   Applicant's arguments with respect to claims 1-5 and 9-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fukumoto et al(US 20030048248) teach a display device comprising a resistor ladder.

Yamaguchi et al(6,476,591) teach a display device comprising a fixed resistor can be replaced by a variable resistor.

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

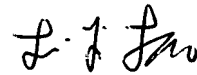Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

August 1, 2007

Lun-yi Lao
Primary Examiner